DESCRIPTION

LAMINATED COIL COMPONENT AND METHOD OF MANUFACTURING THE SAME

Technical Field

The present invention relates to laminated coil components and methods of manufacturing the same. In particular, the present invention relates to conformation of coil conductors inside ceramic laminates.

Background Art

A longitudinally laminated and laterally coiled chip inductor disclosed in Patent Document 1 is an example of a laminated coil component. As shown in Fig. 11, a chip inductor 31 includes a coil conductor 33 having the axis orthogonal to the laminated direction (thickness direction) X inside an approximately rectangular parallelepiped ceramic laminate 32. Namely, the coil conductor 33 having the axis in the longitudinal direction Y of the ceramic laminate 32 is provided inside the ceramic laminate 32. Strip electrodes 34 are disposed at the upper portion and the lower portion inside the ceramic laminate 32. The ends of the strip electrodes 34 are connected with each other inside the ceramic laminate 32 through via-holes 35 passing through the ceramic laminate 32 in the thickness direction X to form the coil conductor 33.

The via-holes 35 are formed by providing through-holes at predetermined positions of each ceramic green sheet constituting the ceramic laminate 32 and by filling these through-holes with a conductive material (conductive paste) such as an Ag paste. An example of the ceramic green sheet is a ferrite sheet. The two endmost strip electrodes 34 disposed at the upper portion of the ceramic laminate 32 extend to the side faces in the longitudinal direction Y of the ceramic laminate 32, and are connected to external

electrodes 37 coated on the side faces of the ceramic laminate 32, respectively.

Regarding the preparation (not shown) of the ceramic laminate 32 of the chip inductor 31, a plurality of ceramic green sheets having via-holes 35 only are stacked in the laminated direction X. Then, a plurality of ceramic green sheets having strip electrodes 34 and via-holes 35 are attacked on the top and the bottom of the resulting laminate of the ceramic green sheets. Furthermore, a plurality of ceramic green sheets without the strip electrodes 34 and the via-holes 35 are stacked on the top and the bottom of the resulting laminate of the ceramic green sheets.

The ceramic laminate 32 is prepared by press-bonding the laminated ceramic green sheets monolithically along the laminated direction X, and by then firing. Then, the external electrodes 37 are formed on the side faces of the ceramic laminate 32 by dipping with a conductive paste and subsequent firing. Thus, the chip inductor 31 having the dipped end faces is prepared.

Patent Document 1: Japanese Unexamined Patent Application Publication No. 2002-252117

Disclosure of Invention

Problems to Be Solved by the Invention

The relative inductance (L) of a coil in a laminated coil component will now be investigated. For example, in the known chip inductor 31, the coil conductor 33 can have the highest relative inductance (L) when the inner cross-sectional area (inner area) and the outer cross-sectional area (outer area) of the coil conductor 33 are the same as each other. Namely, the highest relative inductance (L) can be achieved when the laminated coil component is designed to have a ratio of approximately 1 : 1 regarding these areas.

In the design of the chip inductor 31, some restrictions must be taken into account. The ceramic green sheets stacked for constituting outer coatings on the top position and the bottom position in the thickness direction X of the coil conductor 33 disposed inside the ceramic laminate 32 must have an outer-coating thickness larger than a predetermined level in order to prevent Ag diffusion. Side gaps in the width direction Z of the ceramic laminate 32 must be larger than a minimum gap required in order to prevent the exposure of the strip electrodes 34 and the via-holes 35 to the exterior regardless of distortion during laminating or cutting.

These restrictions are more noticeable as the outside dimension of the chip inductor 31 decreases. As a result, it is highly disadvantageous to design a coil conductor 33 having substantially equal inner area and outer area.

The ceramic laminate 32 of the chip inductor 31 is prepared by press-bonding laminated a large number of ceramic green sheets, and by firing them after cutting. In general, the conductive material in the through-holes constituting the via-holes 35 are not readily deformed during the press-bonding compared with the ceramic green sheets. Therefore, the conductive material functions as posts for resisting the compacting pressure during the press-bonding, and the via-holes 35 receive the compacting pressure.

Consequently, the compacting pressure applied to ceramic regions near the via-holes 35 which are densely aligned is smaller than that applied to ceramic regions far away the via-holes 35. Because of low compacting pressure, delamination and insufficient sintering during firing readily occur at the ceramic regions near the via-holes 35. Furthermore, the conductive material Ag for the via-holes 35 is easily diffused, resulting in a decrease in insulating resistance between the via-holes 35.

The present invention has been made to overcome these

disadvantages. It is an object of the present invention to achieve a high relative inductance (L) by equalizing the inner area and the outer area of a coil conductor, while the small size and the thin shape are maintained. Furthermore, it is an object to provide a laminated coil component which can effectively prevent a decrease in insulating resistance between via-holes and a method for manufacturing the same.

Summary of the Invention

A laminated coil component according to a first aspect of the present invention includes a coil conductor composed of a plurality of strip electrodes and via-holes for connecting predetermined ends of the strip electrodes inside an approximately rectangular parallelepiped ceramic laminate. The axis of the coil conductor corresponds with the width direction of the ceramic laminate orthogonal to both the laminated direction (thickness direction) and the longitudinal direction of the ceramic laminate. Namely, the axis of the coil conductor is orthogonal to the laminated direction (thickness direction) of the ceramic laminate and also orthogonal to the longitudinal direction of the ceramic laminate.

According to a second aspect of the present invention, the laminated coil component recited in the first aspect is characterized that external electrodes are disposed at end regions in the longitudinal direction on a main surface in the laminated direction of the ceramic laminate and are connected to the ends of the coil conductor.

According to a third aspect of the present invention, the laminated coil component recited in the second aspect is characterized that the external electrodes cover the regions where the via-holes are arranged.

A method according to a fourth aspect of the present invention for

manufacturing the laminated coil component described in the third aspect includes the steps of laminating ceramic green sheets having the strip electrodes and/or the via-holes and ceramic green sheets having printed conductive patterns constituting the external electrodes, and press-bonding and firing the laminated ceramic green sheets.

Advantageous Effect of the Invention

In a laminated coil component having a built-in coil conductor, in order to achieve a reduction in size and thickness, particularly, in order to achieve a low profile, the thickness of the laminated coil component is smaller than its length and width. In such a conformation, the inner area of the coil conductor is extremely smaller than the outer area when the axis of the coil conductor corresponds with the longitudinal direction of a ceramic laminate.

The reduction in size and thickness of a laminated coil component according to the present invention is achieved by utilizing general characteristics of the laminated coil component. The laminated coil component according to the present invention can achieve a high relative inductance (L) even if an outer-coating thickness and side gaps are minimized. Accordingly, the bias characteristics are improved and a manufacturing cost is decreased because the number of the via-holes can be reduced compared with that of a known component.

In the laminated coil component described in the first aspect, the axis of the coil conductor corresponds with the width direction of the ceramic laminate orthogonal to both the laminated direction (thickness direction) and longitudinal direction of the ceramic laminate. Therefore, the inner area of the coil conductor is prevented from being extremely smaller than the outer area, and the relative inductance (L) of the coil conductor can be increased by the equality of these areas. Accordingly, the bias characteristics are improved

and a manufacturing cost is decreased because the number of the via-holes can be reduced compared with that of a known component.

In the laminated coil component described in the second aspect, the external electrodes are disposed at end regions in the longitudinal direction on a main surface in the laminated direction of the ceramic laminate and are connected to the ends of the coil conductor. Namely, in this laminated coil component, the external electrodes are disposed on a main surface in the thickness direction, not on the side faces in the longitudinal direction of the ceramic laminate.

In general, the external electrodes of a known laminated coil component are formed by dipping the side faces of the ceramic laminate. The external electrodes have not been disposed on a main surface of the ceramic laminate. In the laminated coil component according to the present invention, since the external electrodes are disposed on a main surface of the ceramic laminate, a process for mounting the laminated coil component on a substrate or the like, i.e. a process for connecting the external electrodes of the laminated coil component to wiring patterns on a substrate is readily performed.

For example, the external electrodes of the laminated coil component and the wiring patterns on the substrate can be readily connected each other by wire-bonding or with a bump disposed between each external electrode of the laminated coil component and each wiring pattern on the substrate. Preferably, the external electrodes are disposed at the inside of the edge of a main surface of the ceramic laminate in order to avoid chipping or delamination during barreling. In such a structure, the stray capacitance is smaller than that of the known product having dipped end faces.

In the laminated coil component described in the third aspect of the present invention, since the external electrodes are disposed so as to cover the regions where the via-holes are arranged, the

compacting pressure during the press-bonding of the ceramic laminate acts not only on the via-holes but also on the ceramic regions near the via-holes through the external electrodes. Therefore, the ceramic regions near the via-holes are also pressed with a compacting pressure equal to that at the ceramic regions far from the via-holes.

Therefore, occurrence of delamination and insufficient sintering during firing can be readily inhibited at the ceramic regions near the via-holes. As a result, Ag diffusion to the ceramic region and a decrease in insulating resistance between the via-holes can be effectively inhibited.

When a mold is used for press-bonding, the surface of the external electrode disposed on a main surface of the ceramic laminate can be formed flat. As a result, for example, a bonding strength for binding a bonding wire to the external electrode is advantageously improved compared with that in the known external electrode formed by dipping.

In the process described in the fourth aspect of the present invention for manufacturing the laminated coil component, ceramic green sheets having the strip electrodes and/or the via-holes and ceramic green sheets having printed conductive patterns constituting the external electrodes are laminated, and then press-bonding and firing are performed. In such a process, the laminated coil component described in the third aspect is readily manufactured.

In such a manufacturing process, after connecting the external electrodes to the coil conductor through the via-holes, the conductive patterns for the external electrodes can also be fired in a process for firing the ceramic laminate. Therefore, in order to form the external electrodes, the coating and firing processes for the conductive paste alone are unnecessary. Therefore, the processing cost is reduced.

Best Mode for Carrying Out the Invention

An object to equalize the inner area and the outer area of a coil conductor to ensure a high relative inductance (L) of the coil conductor while satisfying a reduction in size and thickness of a laminated coil component and to effectively prevent a decrease in insulating resistance between via-holes is achieved by a significantly simple structure and process.

First embodiment

Fig. 1 is a perspective view of an appearance of a chip inductor of a laminated coil component according to a first Embodiment. Fig. 2 is an exploded perspective view of the chip inductor. Fig. 3 is a graph showing characteristics of relative inductance (L) with an applied current. Fig. 4 is a graph showing a rate of change in relative inductance (L) with an applied current. Fig. 5 shows a relationship between a ratio of the areas and bias characteristics in a coil conductor. Figs. 6 to 8 are side views of mounted chip inductors; Fig. 6 shows a first mounting structure, Fig. 7 shows a second mounting structure, and Fig. 8 shows a third mounting structure.

Referring to Fig. 1 showing the appearance and Fig. 2 showing the exploded structure, the chip inductor 1 includes a coil conductor 4 composed of a plurality of strip electrodes 2 and a large number of via-holes 3 inside an approximately rectangular parallelepiped ceramic laminate 5. The via-holes 3 electrically and mechanically connect predetermined ends of the strip electrodes 2. In the chip inductor 1, the strip electrodes 2 are disposed at predetermined intervals at the upper portion and the lower portion in the laminated direction (thickness direction) X of the ceramic laminate 5, and the ends of the strip electrodes 2 are connected with the via-holes 3 passing through the ceramic laminate 5 in the thickness direction X so that the coil conductor 4 is spiral.

In this structure, the axis of the coil conductor 4 corresponds

with the width direction Z of the ceramic laminate 5 orthogonal to both the laminated direction (thickness direction) X and the longitudinal direction Y of the ceramic laminate 5. Namely, the direction of the axis of the coil conductor 4 is orthogonal to the laminated direction X of the ceramic laminate 5 and also orthogonal to the longitudinal direction of the ceramic laminate 5. One of the ends of each strip electrodes 2 aligned at the endmost positions in the width direction Z at the upper position of the ceramic laminate 5 is connected to the via-hole 3 passing through the ceramic laminate 5 in the thickness direction X and extending to the upper main surface in the thickness direction X of the ceramic laminate 5.

Exposed external electrodes 6 are disposed on end positions in the longitudinal direction Y of the upper main surface in the thickness direction X of the ceramic laminate 5. The via-holes 3 extend to the upper main surface of the ceramic laminate 5 and are electrically connected to the respective external electrodes 6. In the chip inductor 1, each of the external electrodes 6 is disposed on the top surface in the laminated direction X of the ceramic laminate 5 to cover the region where the via-holes 3 are aligned.

The strip electrodes 2 and the external electrodes 6 are formed on surfaces of ceramic green sheets 7 constituting the ceramic laminate 5 with a conductive material (conductive paste) such as an Ag paste. In Fig. 2, three-layer strip electrodes 2 are formed; however, only one-layer strip electrodes 2 may be formed. The via-holes 3 are formed, for example, by irradiating each of the ceramic green sheets 7 with a laser beam to provide through-holes at predetermined positions of the ceramic green sheets 7 and then by filling the through-holes with a conductive material such as an Ag paste.

In the embodiment, the external electrodes 6 are each aligned at inner position than the edge of a main surface of the ceramic laminate 5. In this state, the external electrode 6 does not undergo chipping

or delamination during a barreling process. However, the conformation is not limited to such a state. The external electrode 6 may extend to the edge of the main surface of the ceramic laminate 5 (not shown).

In the chip inductor 1, the axis of the coil conductor 4 corresponds with the width direction Z of the ceramic laminate 5 orthogonal to both the laminated direction (thickness direction) X and the longitudinal direction Y of the ceramic laminate 5. The fired chip inductor 1 has a thickness of 0.35 mm, a width of 3.2 mm, an outer-coating thickness of 0.04 mm, and side gaps of 0.1 mm. In such a chip inductor 1, the inner area and the outer area of the coil conductor 4 are very similar, i.e. it was observed by the inventors of the present invention that the ratio of these areas is 1 : 1.4 and the relative inductance (L) of the coil conductor 4 is 1.1 μH.

On the other hand, in a known chip inductor 31, for example, when the fired chip inductor has a thickness of 0.35 mm, a width of 1.6 mm, an outer-coating thickness of 0.04 mm, and side gaps of 0.1 mm, the ratio of the inner area and the outer area of the coil conductor 33 is 1 : 1.8. Therefore, the relative inductance (L) of the coil conductor 33 is only 1.0 μH. It is also observed that the relative inductance (L) of the inventive chip inductor 1 is higher than that of the known chip inductor 31.

The results observed by the inventors on the measurement of inductance (L) characteristics and the rate of change of inductance (L) at the application of a current are shown in Figs. 3 and 4. In Figs. 3 and 4, the solid lines represent the results in the inventive chip inductor 1 and the broken lines represent the results in the known chip inductor 31. As shown in Figs. 3 and 4, the inventive structure is superior to the known structure in both the inductance (L) characteristics and the rate of change of inductance (L).

Fig. 5 shows a relationship between the ratio of the areas and the bias characteristics of the coil conductor 4 at a current level when

the inductance decreases by 30%. Namely, according to the observed results, when the ratio of the inner area and the outer area of the coil conductor 4 is approximately 1 : 1, the upper limit of an allowable current level is higher than that of a coil conductor having a ratio of the areas far from 1 : 1. Therefore, a high inductance is maintained even if a large amount of current is biased. As a result, in the chip inductor 1 having the structure according to the embodiment, the bias characteristics can be improved while a high relative inductance (L) is maintained, even if the outer-coating thickness and side gaps are minimized.

Furthermore, in the chip inductor 1, the external electrodes 6 are disposed on a main surface of the ceramic laminate 5 and cover the regions where the via-holes 3 are disposed in the ceramic laminate 5. Therefore, during the press-bonding of the ceramic laminate 5, a compacting pressure for the press-bonding acts not only on the via-holes 3 but also on ceramic regions near the via-holes 3 through the external electrodes. As a result, the ceramic regions among the via-holes 3 can be sufficiently press-bonded and the occurrence of delamination and insufficient sintering during firing of the ceramic laminate 5 can be prevented.

The inventors of the present invention investigated the relationship between a thickness of the external electrodes 6 disposed on a main surface of the ceramic laminate 5 and the rate of delamination. The rate of delamination was 15% when the external electrodes 6 are not formed on the main surface of the ceramic laminate 5.

On the other hand, when the external electrodes 6 are formed by printing at a thickness of 5 μm so as to have a thickness of 3 μm after the press-bonding, the rate of delamination was 10%. When the external electrodes 6 are formed by printing at a thickness of 15 μm so as to have a thickness of 10 μm after the press-bonding, the rate

of delamination was 0%. It was observed that the rate of delamination is significantly improved by the presence of the external electrodes 6. In particular, it is preferable that the external electrodes 6 be printed at a thickness of 15 μm or more.

If delamination and insufficient sintering during firing of the ceramic laminate 5 can be prevented, Ag diffusion to the ceramic regions among the via-holes 3 and a decrease in insulating resistance between the via-holes are efficiently prevented. When the ceramic laminate 5 is press-bonded with a mold (not shown), external electrodes 6 having flat surfaces are formed. As a result, for example, the bonding strength between a bonding wire and the external electrode 6 is advantageously improved.

The inventors of the present invention compared the bonding strength of the external electrodes 6 plated with Ni (base) and Au on the main surface of the ceramic laminate 5 in the chip inductor 1 with the bonding strength of the external electrodes 37 plated with Ni (base) and Au on the side faces of the ceramic laminate 32 by dipping and firing in the known chip inductor 31. Namely, Au-wire bonding in these chip inductors was evaluated by a ball shear test and a wire pull test. The results of these tests showed that the chip inductor 1, i.e. the structure having the external electrodes 6 plated with Ni (base) and Au on the main surface of the ceramic laminate 5, has a bonding strength higher than that of the other.

When the external electrodes 6 are disposed at regions near the edges in the longitudinal direction Y of the upper main surface in the thickness direction X of the ceramic laminate 5 in the chip inductor 1, various structures for mounting can be employed as described below. In a first mounting structure shown in Fig. 6, each of the external electrodes 6 of the chip inductor 1 and a wiring pattern 8 on a substrate on which the chip inductor 1 is mounted are readily bonded by wire bonding with an Au wire 9 or the like.

In a second mounting structure shown in Fig. 7, solder balls or Au balls 10 may be used for bonding. In this case, the solder balls or Au balls 10 are provided on the external electrodes 6 of the chip inductor 1, and are then bonded to the external electrodes 6 by reflowing or an ultrasonic treatment. Then, the chip inductor 1 is turned upside down and then each of the solder balls or Au balls 10 is bonded to a wiring pattern 8 on a substrate by reflowing or the like.

In a third mounting structure shown in Fig. 8, each of the Au-plated external electrodes 6 of the chip inductor 1 and a wiring pattern 8 on a substrate may be directly connected, and then bonded by an ultrasonic treatment. Each of the external electrodes 6 of the chip inductor 1 and the wiring pattern 8 on the substrate on which the chip inductor 1 is mounted can be bonded with a conductive adhesive or anisotropic conductive tape (not shown). In such a mounting structure, since a high temperature by soldering is not applied to the chip inductor 1, the chip inductor 1 does not undergo a change in the characteristics.

A method for manufacturing the chip inductor 1 will now be described with reference to Fig. 2. A water-based binder (vinyl acetate, water-soluble acrylic resin, etc.) or an organic binder (polyvinyl butyral, etc.) is added to a magnetic material, i.e. Ni-Cu-Zn ferrite. After the addition of a dispersant and antifoam, ceramic green sheets 7 are formed by doctor blading or with a reverse-roll coater. A predetermined number of the ceramic green sheets 7 are irradiated with a laser beam at predetermined positions of each ceramic green sheet 7 to form the through-holes for the via-holes 3.

The via-holes 3 are formed by filling the through-holes provided to the ceramic green sheets 7 with an Ag paste by screen-printing. The strip electrodes 2 constituting parts of the coil conductor 4 are formed on predetermined positions of the surface of each ceramic green sheet 7 by screen-printing an Ag paste. Conductive patterns

constituting the external electrodes 6 are formed at predetermined positions on the surfaces of other ceramic green sheets 7.

A predetermined number of the ceramic green sheets 7 having the via-holes 3 only are stacked in the laminated direction X. Then, a predetermined number of the ceramic green sheets 7 having the strip electrodes 2 and the via-holes 3 are stacked on the top and the bottom of the resulting laminate of the ceramic green sheets 7. Furthermore, the ceramic green sheets 7 having the conductive patterns constituting the external electrodes 6 are stacked on the top of the resulting laminate of the ceramic green sheets 7. The ceramic green sheets 7 without any of the strip electrodes 2, the via-holes 3, and the conductive patterns constituting the external electrodes 6 are also stacked on the bottom of the resulting laminate of the ceramic green sheets 7.

A sheet laminate 11 formed in such a process is press-bonded in the laminated direction X, and are then cut into a predetermined size. Then, the ceramic laminate 5 is prepared by degreasing and firing. Subsequently, the external electrodes 6 are formed by Ni plating (base) and Au plating on the conductive patterns constituting the external electrodes 6 to complete the chip inductor 1. The plating may be performed with Ni (base) and Sn instead of Ni (base) and Au. The pressure during the press-bonding of the sheet laminate 11 ranges from 98 MPa to 120 MPa (from 1.0 t/cm^2 to 1.2 t/cm^2).

In this manufacturing process, after the connecting the conductive patterns for the external electrodes 6 to the coil conductor 4 through the via-holes 3, the conductive patterns for the external electrodes 6 can be fired in a process for firing the ceramic laminate 5. Therefore, in order to form the external electrodes 6, the coating and firing processes for the conductive paste alone are unnecessary.

In a laminated coil component according to the embodiment, the chip inductor 1 is provided with one coil conductor 4 inside the

ceramic laminate 5. However, the laminated coil component according to the present invention is not limited to the above-mentioned chip inductor 1. Namely, a plurality of coil conductors 4 may be aligned in parallel inside the ceramic laminate 5. The chip inductor having such a structure is used as a transformer or a common mode choke coil. Furthermore, the present invention can be applied to other laminated coil components such as a multilayer impedor and a multilayer LC filter.

Second embodiment

Fig. 9 is a perspective view of an appearance of a chip inductor according to a second embodiment of the present invention. Fig. 10 is an exploded perspective view of the chip inductor. The chip inductor is represented by reference numeral 21. The structure of the chip inductor 21 according to this embodiment is substantially the same as that of the chip inductor 1 according to the first embodiment except for the structure of the external electrodes.

Therefore, in Figs. 9 and 10, the same elements which are the same as those in Figs. 1 and 2 are referred to with the same reference numerals as in Figs, 1 and 2, and the detailed description of these parts are omitted. Since the manufacturing process and the function of the chip inductor 21 according to the second embodiment are also substantially the same as those of the chip inductor 1 according to the first embodiment, the detailed description is omitted here.

The chip inductor 21 has a similar appearance and exploded structure to those of the chip inductor 1 as shown in Figs. 9 and 10. Namely, the chip inductor 21 includes a coil conductor 4 composed of a plurality of strip electrodes 2 and a large number of via-holes 3 inside an approximately rectangular parallelepiped ceramic laminate 22. The via-holes 3 electrically and mechanically connect predetermined ends of the strip electrodes 2. The axis of the coil conductor 4

corresponds with the width direction Z of the ceramic laminate 22 orthogonal to both the laminated direction (thickness direction) X of the ceramic laminate 22 and the longitudinal direction Y of the ceramic laminate 22.

One of the ends of each strip electrodes 2 aligned at the endmost positions in the width direction Z at the upper position of the ceramic laminate 22 is connected to the via-hole 3 passing through the ceramic laminate 22 in the thickness direction X and extending to the upper main surface in the thickness direction X of the ceramic laminate 22. External electrodes 23 are disposed at the side positions in the longitudinal direction Y of the upper main surface in the thickness direction X of the ceramic laminate 22.

Each of the external electrodes 23 includes a pair of top electrodes 24 apart from each other and a bottom electrode 25 directly below the top electrodes 24. The top electrodes 24 and the bottom electrode 25 are connected through the via-holes 3. The external electrodes 23 are disposed on the top surface in the laminated direction X of the ceramic laminate 22 to cover the regions where the via-holes 3 are aligned.

A method for manufacturing the chip inductor 21 will now be described with reference to Fig. 10. Ceramic green sheets 7 are formed first. Then, through-holes for the via-holes 3 are formed at predetermined positions of a predetermined number of the ceramic green sheets 7. Subsequently, the through-holes are filled with an Ag paste by screen-printing to form via-holes 3. Strip electrodes 2 constituting parts of a coil conductor 4 are formed at predetermined positions on each surface of the ceramic green sheets 7 by screen-printing an Ag paste.

Conductive patterns constituting the top electrodes 24 and the bottom electrodes 25 of the external electrodes 23 are formed at predetermined positions on the surfaces of other ceramic green sheets

7. A predetermined number of the ceramic green sheets 7 having the via-holes 3 only are stacked in the laminated direction X. Then, a predetermined number of the ceramic green sheets 7 having both the strip electrodes 2 and the via-holes 3 are stacked on the top and the bottom of the resulting laminate of the ceramic green sheets 7.

Furthermore, the ceramic green sheet 7 having the conductive patterns constituting the bottom electrodes 25 of the external electrodes 23 is stacked on the top of the resulting laminate of the ceramic green sheets 7. Then, the ceramic green sheet 7 having the conductive patterns constituting the top electrodes 24 of the external electrodes 23 is stacked on the top of the resulting laminate of the ceramic green sheets 7. On the other hand, on the bottom of the resulting laminate of the ceramic green sheets 7, the ceramic green sheets 7 without any of the strip electrodes 2, the via-holes 3, and the conductive patterns for the top electrodes 24 and the bottom electrodes 25 of the external electrodes 6 are stacked.

A sheet laminate 27 formed in such a process is press-bonded along the laminated direction X, and is then cut into a predetermined size. Then, the ceramic laminate 22 is prepared by degreasing and firing. Subsequently, the external electrodes 23 are formed by plating the conductive patterns constituting the top electrode 24 of the external electrodes 23 with Ni (base) and Au to complete the chip inductor 21 having an appearance shown in Fig. 9. Since the Au-plated region of the chip inductor 21 having such a structure is narrower than that of the chip inductor 1 according to the first embodiment, a manufacturing cost can be reduced.

Industrial Applicability

The laminated coil component is not limited to chip inductor. A laminated coil component having two or more coil conductors arranged in parallel inside a ceramic laminate may be used in a transformer and

a common-mode choke coil. Furthermore, the present invention can be applied to other laminated coil components such as multilayer impedors and multilayer LC filters.

Brief Description of the Drawings

Fig. 1 is a perspective view of an appearance of a chip inductor of a laminated coil component according to a first embodiment of the present invention.

Fig. 2 is an exploded perspective view of the chip inductor.

Fig. 3 is a graph showing relationships between inductance (L) characteristics and applied current.

Fig. 4 is a graph showing rates of change of inductance (L) with applied current.

Fig. 5 shows a relationship between a ratio of the areas of a coil conductor and bias characteristics.

Fig. 6 is a side view of a first mounting structure of the chip inductor.

Fig. 7 is a side view of a second mounting structure of the chip inductor.

Fig. 8 is a side view of a third mounting structure of the chip inductor.

Fig. 9 is a perspective view of an appearance of a chip inductor of a laminated coil component according to a second embodiment of the present invention.

Fig. 10 is an exploded perspective view of the chip inductor.

Fig. 11 is a perspective view of an appearance of a chip inductor of a laminated coil component according to a known example.

Reference Numerals

1 chip inductor (laminated coil component)

2 strip electrode

3 via-hole

4 coil conductor

5 ceramic laminate

6 external electrode

7 ceramic green sheet

21 chip inductor (laminated coil component)

22 ceramic laminate

23 external electrode

X laminated direction (thickness direction) of ceramic laminate

Y longitudinal direction of ceramic laminate

Z width direction of ceramic laminate